UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,428	12/28/2001	William H. Moody II	CROSS1510	1923

25094 7590 08/04/2005

DLA PIPER RUDNICK GRAY CARY US, LLP
2000 University Avenue
E. Palo Alto, CA 94303-2248

EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,428	MOODY, WILLIAM H.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31,32,38-41,43,44,49-52 and 56-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31,32,38-41,43,44,49-52 and 56-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to the amendment filed 18 May 2005.

2. Applicant's arguments with respect to claims 31 and 43 have been fully considered but they are not persuasive. The rejection of claims 31 and 43 is given below.

3. Applicant's arguments with respect to claims 38, 39, 49 and 50 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 31, 32, 43 and 44 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Contrary to the limitation in claims 31 and 43 that the secondary component continues operating if the first identifier is not compatible with the second identifier, the specification teaches that the secondary component is disabled (fig. 3, disable module; paragraphs 22 and 27). Claims 43 and 44 depend, respectively, on claims 31 and 43.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 38, 39, 43, 49, 50 and 56 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 38 and 39 recite the limitation "the non-volatile memory" in line 12. Claims 49 and 50 recite the limitation "the non-volatile memory" in line 15. Claim 43 recites the limitation "a second ide primary component" in lines 5-6. Claim 56 recites the limitation "the first interface" in line 6. There is insufficient antecedent basis for these limitations in the claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 39 and 50 are rejected under 35 U.S.C. 102(e) as being anticipated by Goers et al., U.S. Patent No. 6,661,236 ("Goers").

As per claim 39, Goers teaches a method comprising:

providing a primary electronic component having a first identifier, wherein the first identifier includes branding information corresponding to the primary electronic component (fig. 1, base unit 1 and interface 3; col. 4, lines 1-4; col. 5, lines 56-67, signal processing means 12 inherently has first identifier in order to perform step 506);

providing a secondary electronic component having a second identifier stored therein, wherein the second identifier includes branding information corresponding to the secondary electronic component (fig. 1, pluggable electrical unit 2 with ROM 21);

coupling the secondary component to the primary component wherein coupling the secondary component to the primary component comprises coupling the secondary component to the primary component via a first interconnect which is configured to transfer data between the secondary component and the primary component during normal operation and via a second interconnect which is configured to transfer data between the *secondary component* and the primary component for the purposes of comparing the first identifier to the second identifier and wherein the second interconnect is an Inter-IC bus (fig. 1, via module bus 43" and identification bus 41"; col. 3, lines 61-67);

comparing the first identifier to the second identifier (fig. 2, step 506);

operating the primary component in conjunction with the secondary component if the first identifier is compatible with the second identifier (fig. 2, steps 507-510); and

operating the primary component without the secondary component if the first identifier is not compatible with the second identifier (fig. 2, steps 550-552).

As per claim 50, Goers teaches a system comprising:

a primary electronic component having a first identifier, wherein the first identifier includes branding information corresponding to the primary electronic component (fig. 1, base unit 1 and interface 3; col. 4, lines 1-4; col. 5, lines 56-67, signal processing means 12 inherently has first identifier in order to perform step 506); and

a secondary electronic component having a second identifier stored therein, wherein the second identifier includes branding information corresponding to the secondary electronic component, the secondary component is configured to be coupled to the primary component (fig. 1, pluggable electrical unit 2 with ROM 21), the primary component is configured to compare the first identifier to the second identifier, the primary component is configured to enable operation in conjunction with the secondary component if the first identifier is compatible with the second identifier and operate without secondary component if the first identifier is not compatible with the second identifier (fig. 2, steps 506, 507-510 and 550-552; col. 6, lines 1-26), the secondary component to the primary component via a first interconnect which is configured to transfer data between the secondary component and the primary component during normal operation and via a second interconnect which is configured to transfer data between the *secondary component* and the primary component for the purposes of comparing the first identifier to the second identifier and wherein the second interconnect is an Inter-IC bus (fig. 1, via module bus 43" and identification bus 41" ; col. 3, lines 61-67).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 38, 48 and 56-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goers et al., U.S. Patent No. 6,661,236 ("Goers"), in view of Locker et al., U.S. Patent No. 6,477,603 ("Locker").

As per claim 38, Goers teaches a method comprising:

providing a primary electronic component having a first identifier, wherein the first identifier includes branding information corresponding to the primary electronic component (fig. 1, base unit 1 and interface 3; col. 4, lines 1-4; col. 5, lines 56-67, signal processing means 12 inherently has first identifier in order to perform step 506);

providing a secondary electronic component having a second identifier stored therein, wherein the second identifier includes branding information corresponding to the secondary electronic component (fig. 1, pluggable electrical unit 2 with ROM 21);

coupling the secondary component to the primary component wherein coupling the secondary component to the primary component comprises coupling the secondary component to the primary component via a first interconnect which is configured to transfer data between the secondary component and the primary component during normal operation and via a second interconnect which is configured to transfer data between the *secondary component* and the primary component for the purposes of comparing the first identifier to the second identifier (fig. 1, via module bus 43" and identification bus 41");

comparing the first identifier to the second identifier (fig. 2, step 506);

operating the primary component in conjunction with the secondary component if the first identifier is compatible with the second identifier (fig. 2, steps 507-510); and

operating the primary component without the secondary component if the first identifier is not compatible with the second identifier (fig. 2, steps 550-552).

However, Goers does not expressly teach that the first interconnect is a PCI bus. Locker teaches PCI as a well-known protocol for a module bus that is used in conjunction with an

identification bus (figs 1-3, PCI Bus 208; col. 3, lines 27-37). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Locker's PCI bus to Goers' first interconnect, as the PCI Specification is well-known in the art.

As per claim 48, Goers teaches a system comprising:

a primary electronic component having a first identifier, wherein the first identifier includes branding information corresponding to the primary electronic component (fig. 1, base unit 1 and interface 3; col. 4, lines 1-4; col. 5, lines 56-67, signal processing means 12 inherently has first identifier in order to perform step 506); and

a secondary electronic component having a second identifier stored therein, wherein the second identifier includes branding information corresponding to the secondary electronic component, the secondary component is configured to be coupled to the primary component (fig. 1, pluggable electrical unit 2 with ROM 21), the primary component is configured to compare the first identifier to the second identifier, the primary component is configured to enable operation in conjunction with the secondary component if the first identifier is compatible with the second identifier and operate without secondary component if the first identifier is not compatible with the second identifier (fig. 2, steps 506, 507-510 and 550-552; col. 6, lines 1-26), the secondary component to the primary component via a first interconnect which is configured to transfer data between the secondary component and the primary component during normal operation and via a second interconnect which is configured to transfer data between the *secondary component* and the primary component for the purposes of comparing the first identifier to the second identifier (fig. 1, via module bus 43" and identification bus 41").

However, Goers does not expressly teach that the first interconnect is a PCI bus. Locker teaches PCI as a well-known protocol for a module bus that is used in conjunction with an identification bus (figs 1-3, PCI Bus 208; col. 3, lines 27-37). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Locker's PCI bus to Goers' first interconnect, as the PCI Specification is well-known in the art.

As per claim 56, Goers teaches an electrical component configured to have a secondary component coupled thereto (fig. 1, base unit 1 coupled to pluggable electrical unit 2), wherein the electrical component comprises:

a functional portion (fig.1, power supply 11);

an interface configured to couple the functional portion to a secondary component (fig. 1, interface 3; col. 4, lines 1-4);

a first identifier includes branding information corresponding to the electrical component (col. 5, lines 56-67, signal processing means 12 inherently has first identifier in order to perform step 506); and

a comparator configured to receive a second identifier, including branding information corresponding to the second component, from the secondary component and to compare the first identifier to the second identifier, wherein the comparator is configured to enable operation in conjunction with the secondary component if the first identifier is compatible with the second identifier and operate without the secondary component if the first identifier is not compatible with the second identifier (fig. 1, signal processing 12; fig. 2, steps 506, 507-510 and 550-552; col. 5, lines 56-67; col. 6, lines 1-26).

Goers teaches a non-volatile memory for storing the second identifier (fig. 1, ROM 21; col. 3, lines 56-60), but doe not expressly teach a counterpart non-volatile memory for storing the first identifier. At the time of the invention, it would have been obvious to one of ordinary skill in the art to implement such a counterpart non-volatile memory, so as to retain information in the electrical component.

While Goers teaches the interface comprises a first interconnect (fig. 1, module bus 43"), Goers does not expressly teach that the first interconnect is a PCI bus. Locker teaches PCI as a well-known protocol for a module bus that is used in conjunction with an identification bus (figs 1-3, PCI Bus 208; col. 3, lines 27-37). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Locker's PCI bus to Goers' first interconnect, as the PCI Specification is well-known in the art.

As per claim 57, Goers teaches a serial bus configured to be coupled to the secondary component, wherein the electrical component is configured to receive the second identifier via the serial bus (fig. 1, identification bus 41").

As per claim 58, Goers teaches the serial bus comprises an Inter-IC bus (col. 3, lines 61-67).

8. Claims 40, 41, 51 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goers et al., U.S. Patent No. 6,661,236 ("Goers"), as applied to claims 39 and 50 above, and further in view of SBS Implementers Forum, "System Management Bus (SMBus) Specification", Version 2.0, 3 August 2000 ("SBS").

As per claims 40 and 51, Goers does not expressly teach the first identifier and the second identifier are OEM identities. SBS teaches SMBus is based on Inter-IC protocol (sec. 1.1) and is used to check OEM identities (secs. 5.6.1 & 5.6.3.11-12). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply SBS's checking OEM identities to Goers' method and system, as checking OEM identities is standard procedure.

As per claims 41 and 52, SBS teaches comparing identifiers during boot-up (secs. 3.1.4.2 & 5.6.3.11-12).

9. Claims 59-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goers/Locker, as applied to claims 38 and 49 above, and further in view of SBS Implementers Forum, "System Management Bus (SMBus) Specification", Version 2.0, 3 August 2000 ("SBS").

As per claims 60 and 61, Goers does not expressly teach the first identifier and the second identifier are OEM identities. Locker teaches using an SMBus to check an identifier (fig. 3). SBS teaches SMBus is based on Inter-IC protocol (sec. 1.1) and is used to check OEM identities is standard procedure (secs. 5.6.1 & 5.6.3.11-12). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply SBS's checking OEM identities to Goers' method and system, as checking OEM identities is standard procedure.

As per claims 59 and 62, SBS teaches comparing identifiers during boot-up (secs. 3.1.4.2 & 5.6.3.11-12).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AW